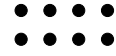
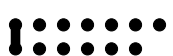
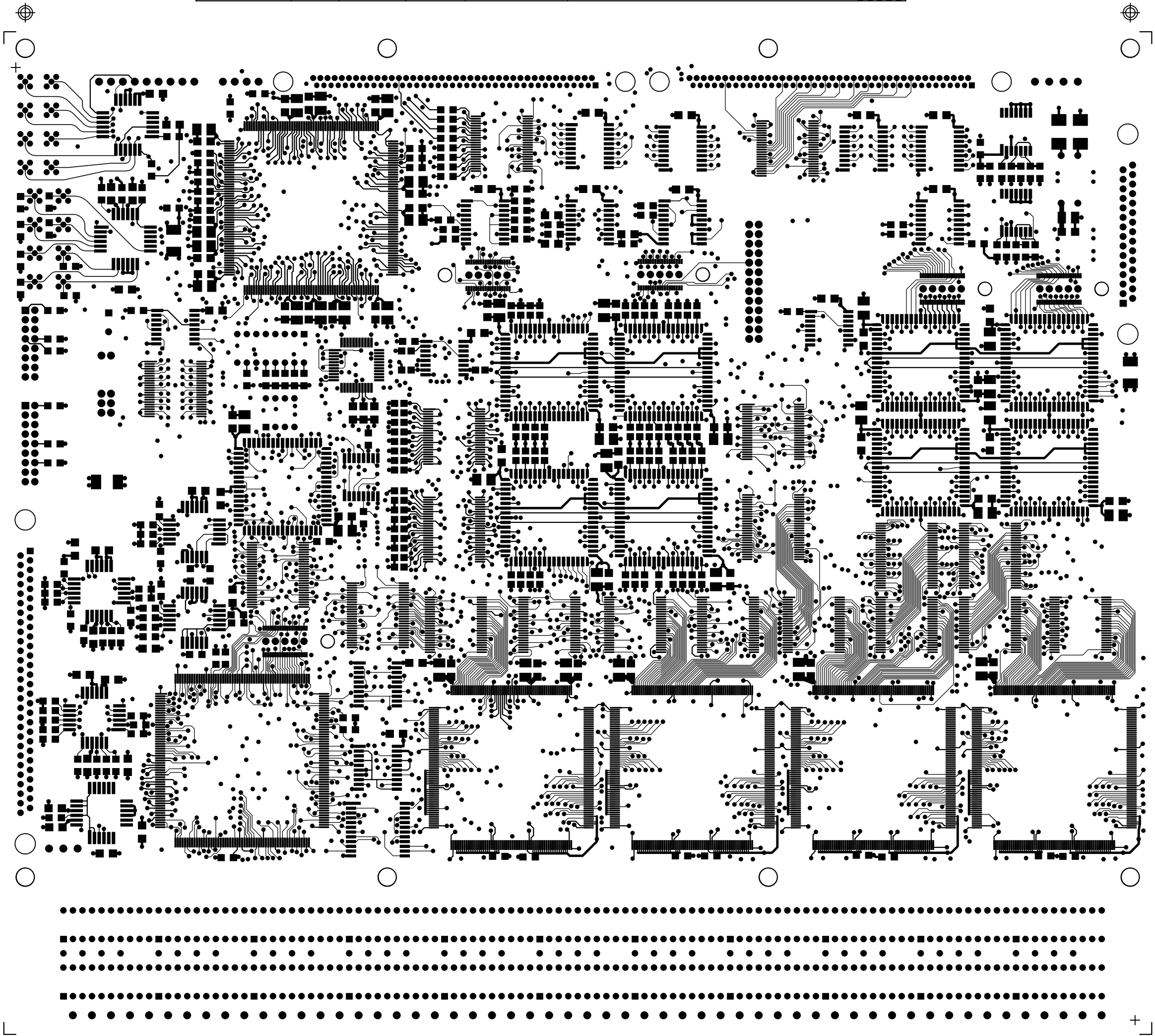


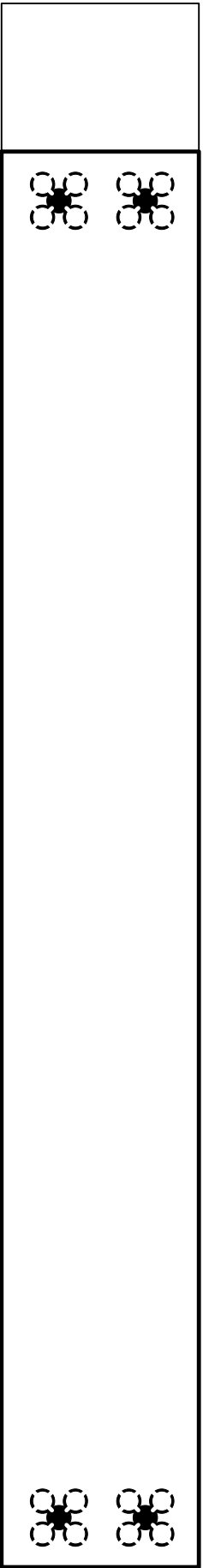
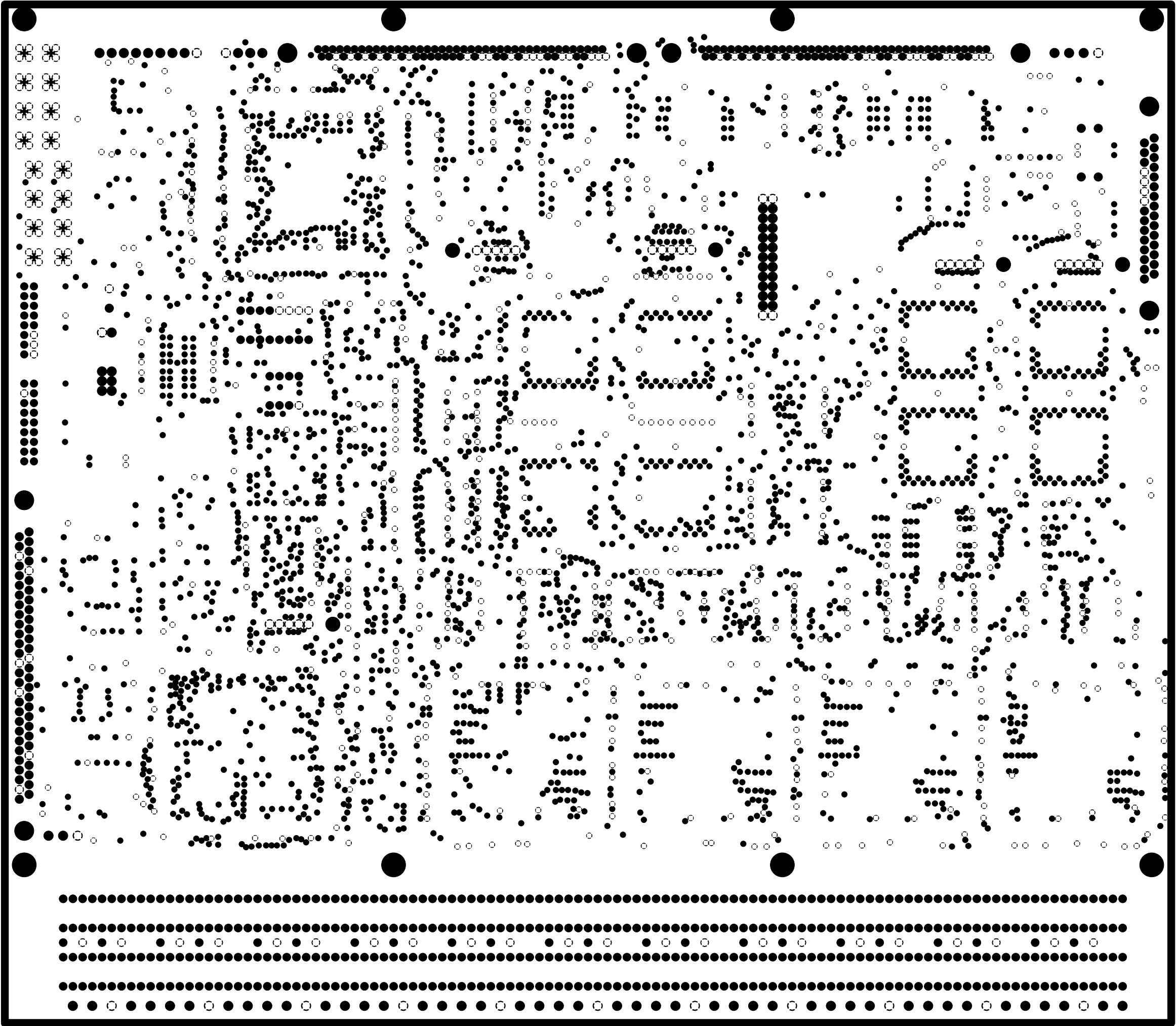
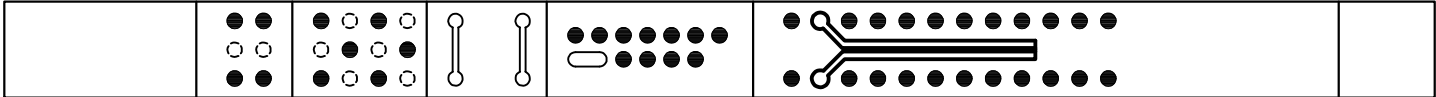
### REV #						LOT	
S/N:	A	B	C	D	E	DATE	



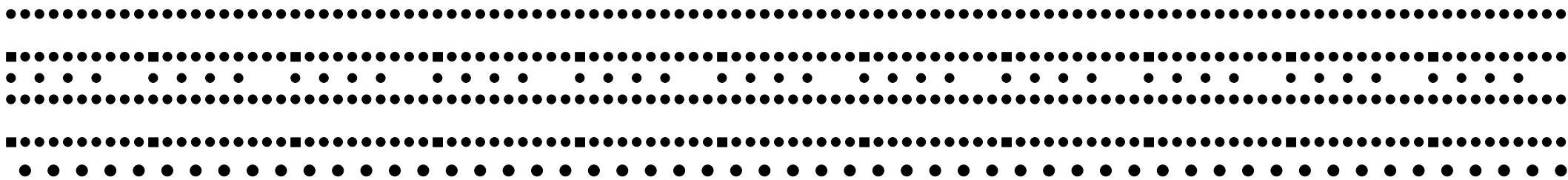
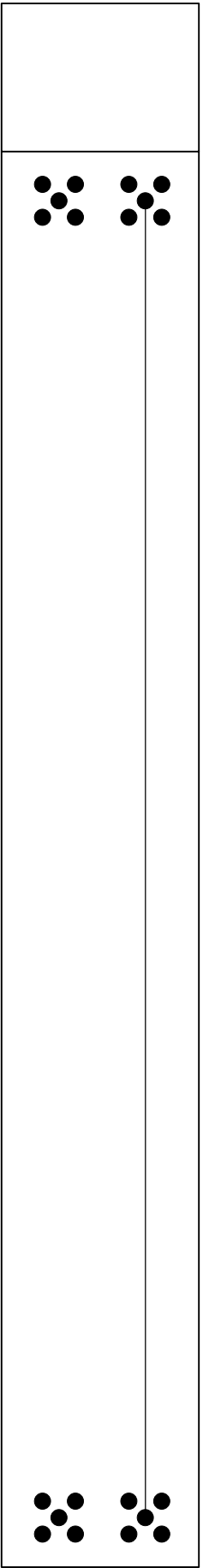
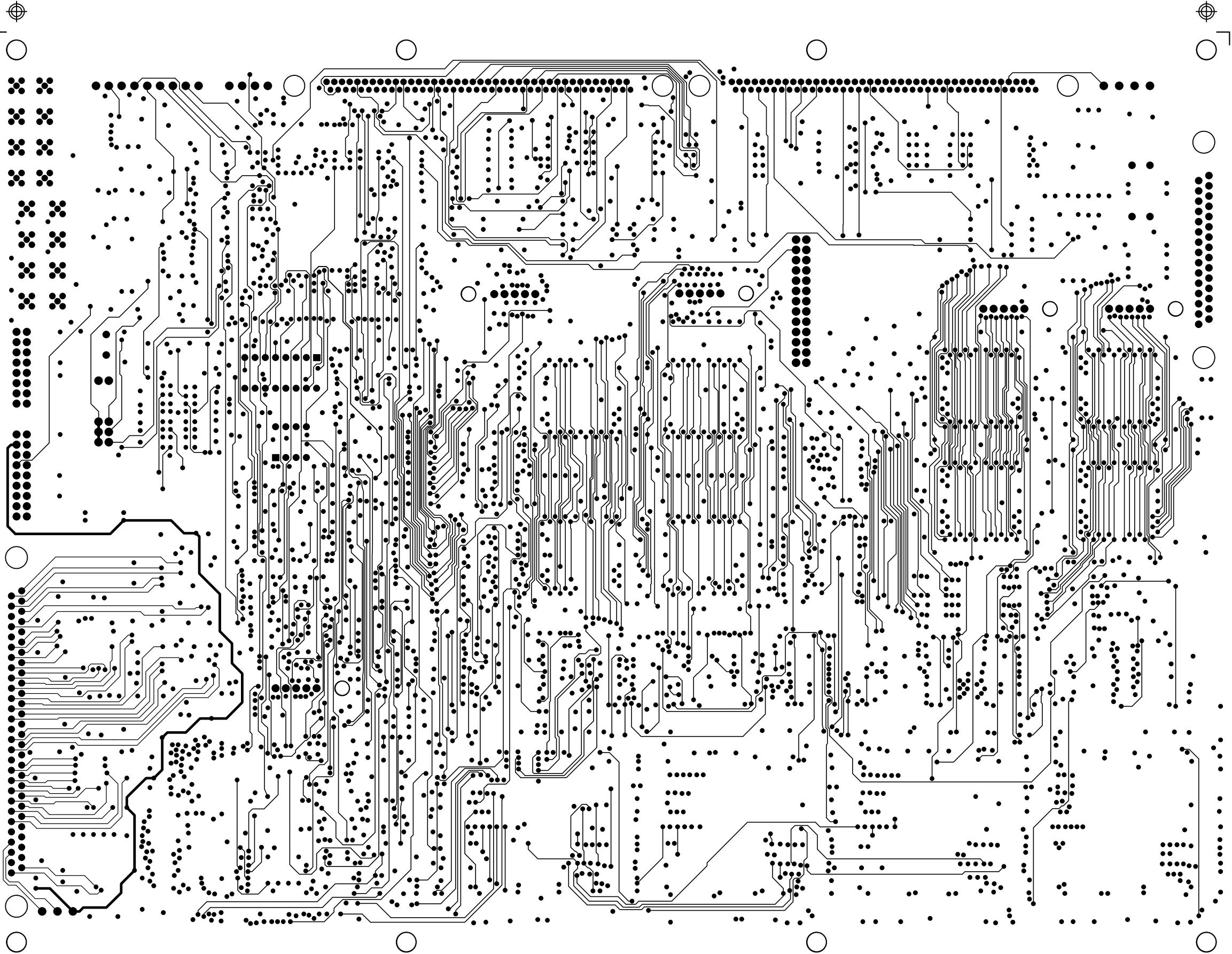
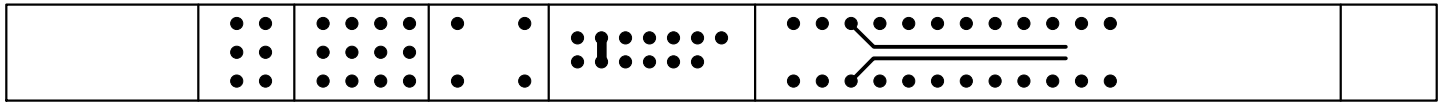
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S/N:	
LAYER 3 50 OHMS	
LAYER 1 50 OHMS	



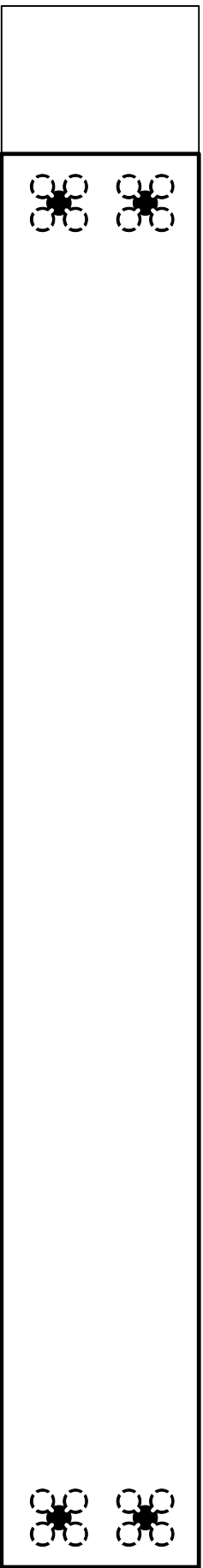
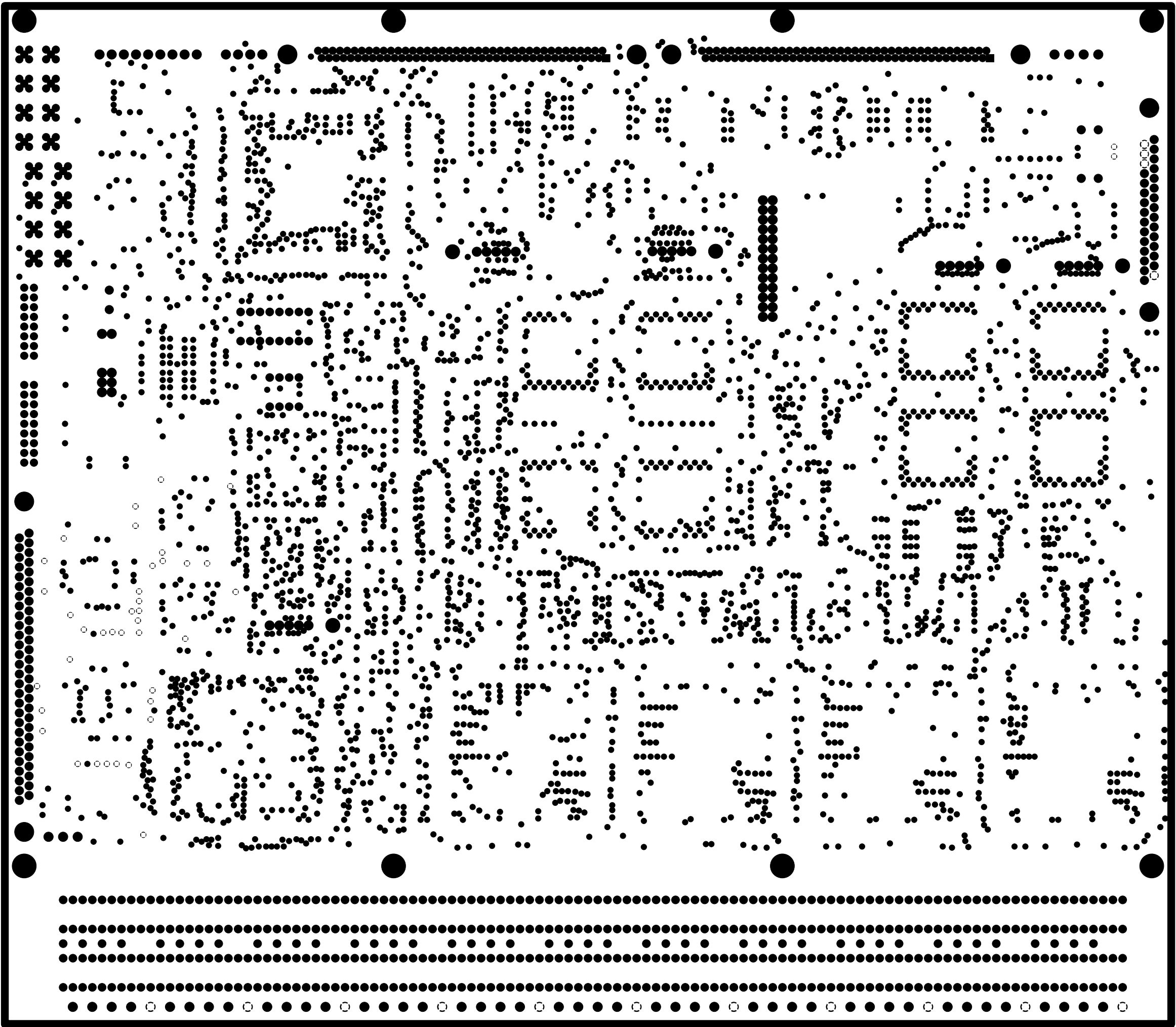
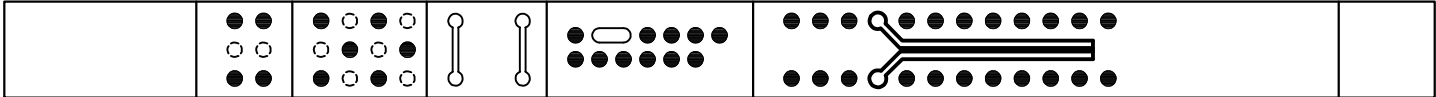
YOUR COMPANY NAME			
ARTWORK / PRIMARY SIDE / LAYER 1			
TEST BOARD			
		NO.	#####
DATE: ###/###/##	REV. #	ARTWORK MASTER L1	



YOUR COMPANY NAME		
ARTWORK / IMBEDDED PLANE (GND) / LAYER 2		
TEST BOARD		
		NO. #####
DATE: ##/##/##	REV. #	ARTWORK MASTER L2



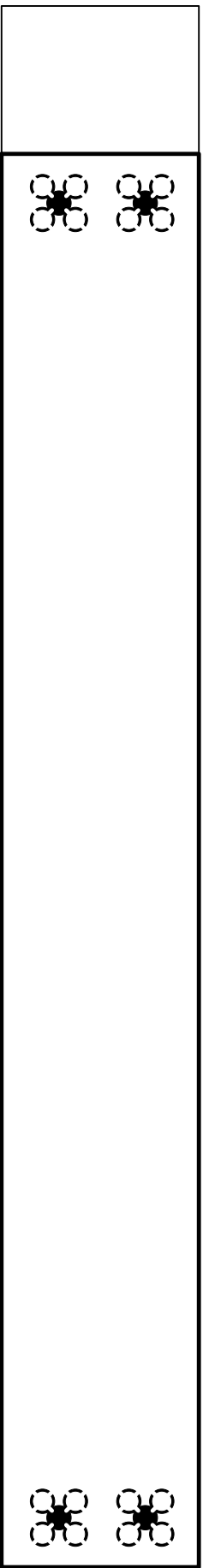
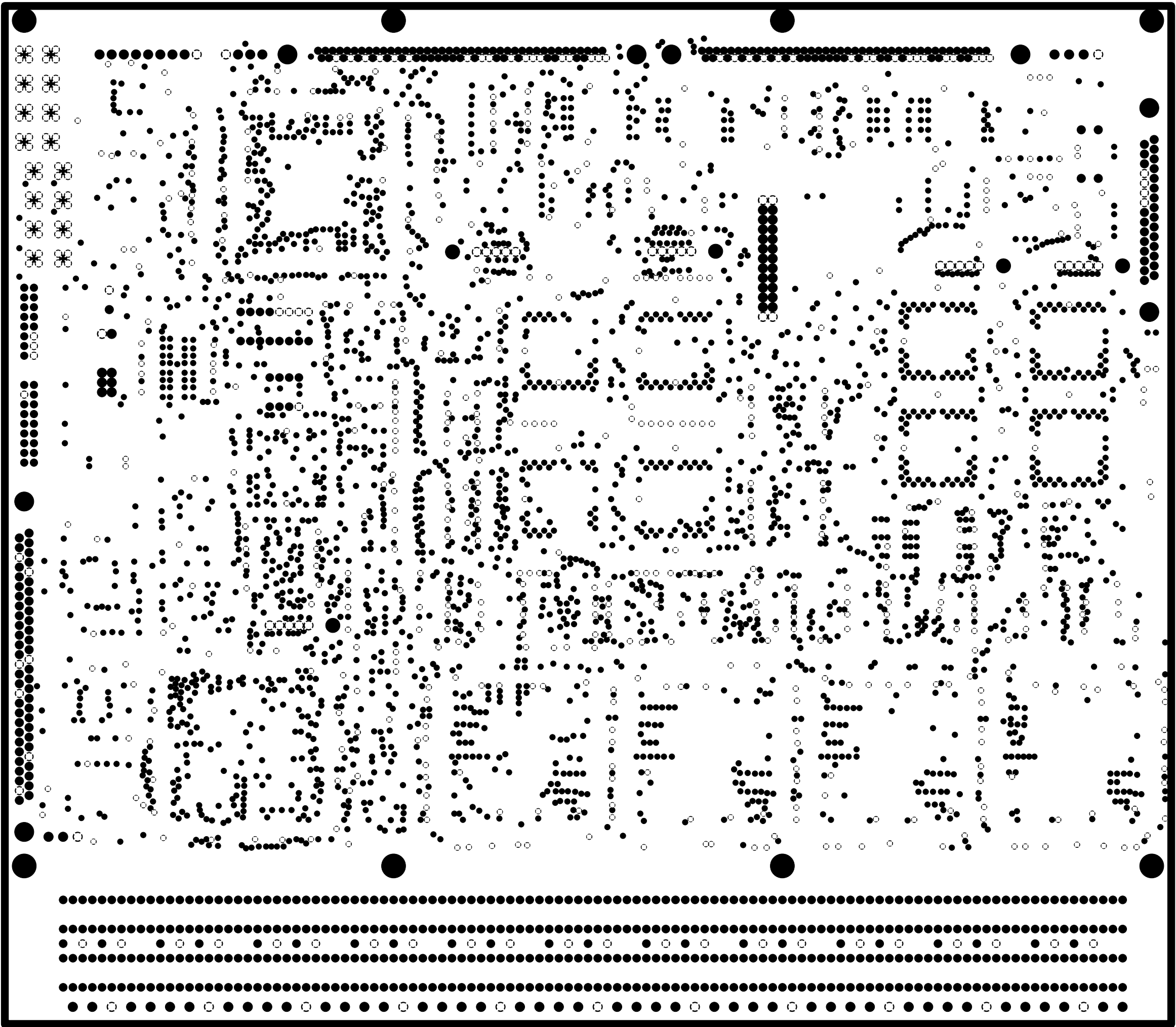
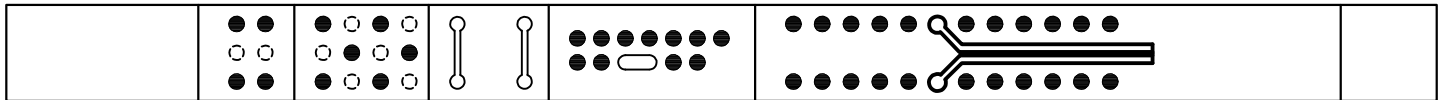
YOUR COMPANY NAME			
ARTWORK / INTERNAL SIGNAL / LAYER 3			
TEST BOARD			
		NO.	#####
DATE: ##/##/##	REV. #	ARTWORK MASTER L3	



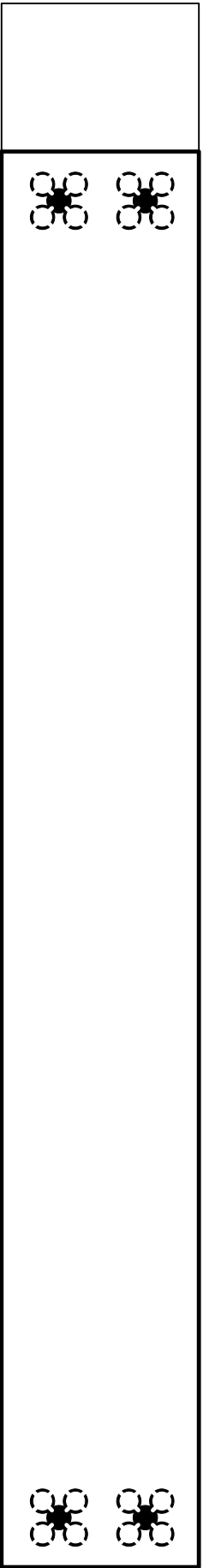
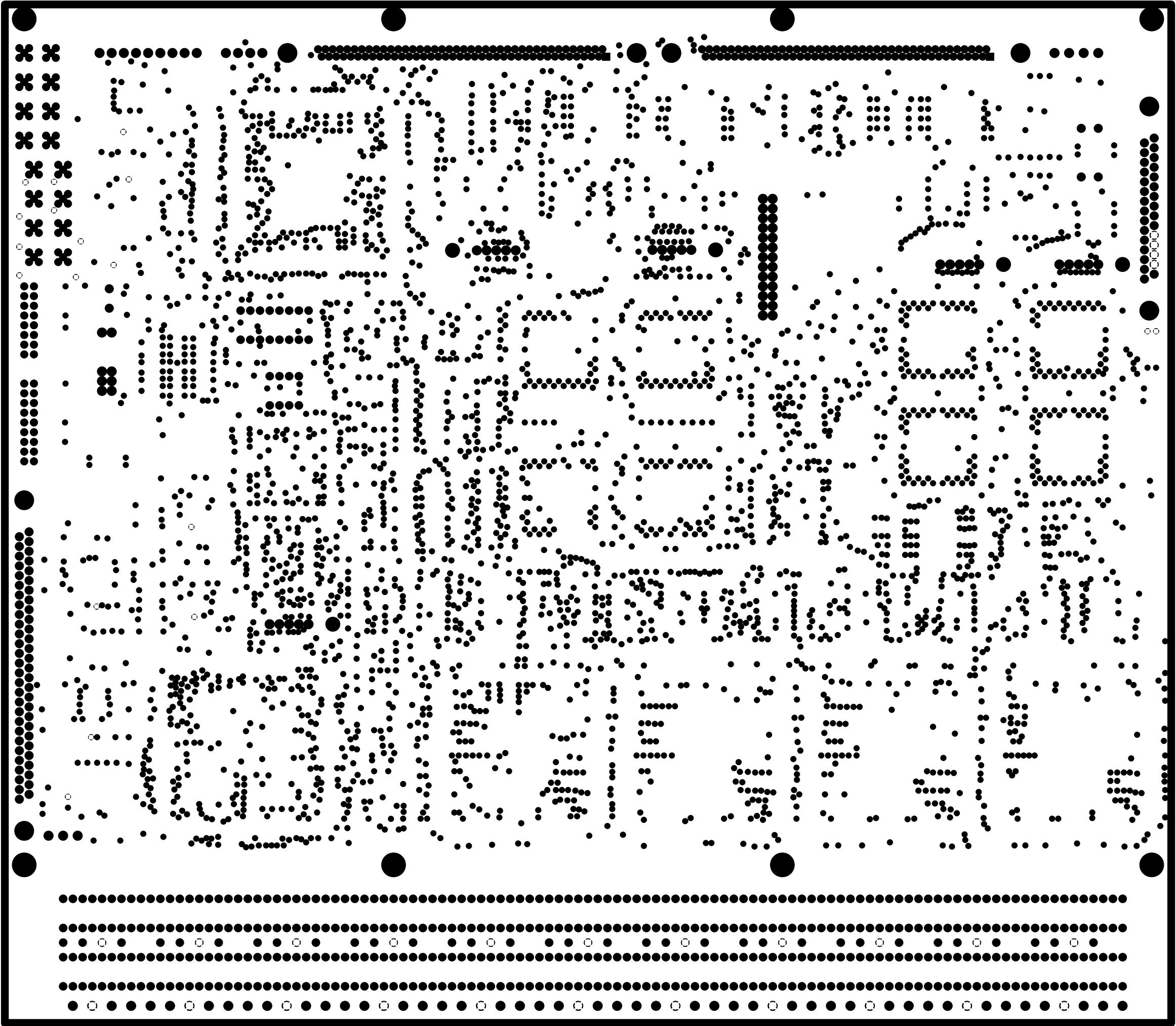
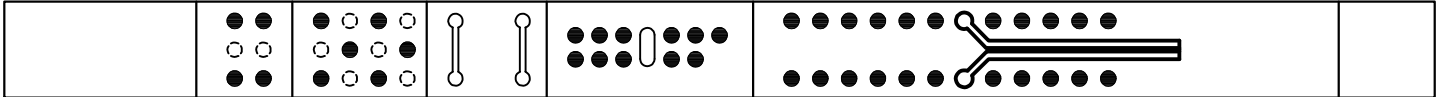
YOUR COMPANY NAME			
ARTWORK / IMBEDDED PLANE (VTT M2 2V) / LAYER 4			
TEST BOARD			
		NO.	#####
DATE: ##/##/##	REV. #	ARTWORK MASTER L4	

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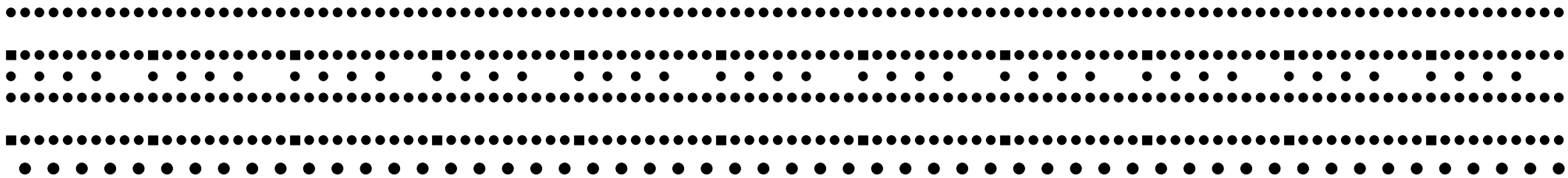
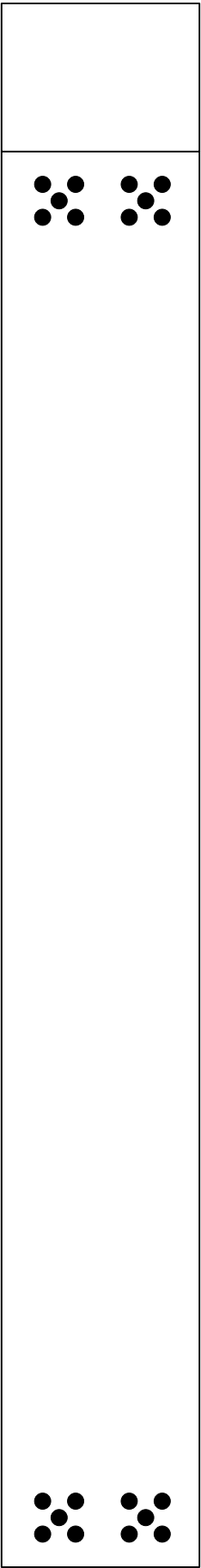
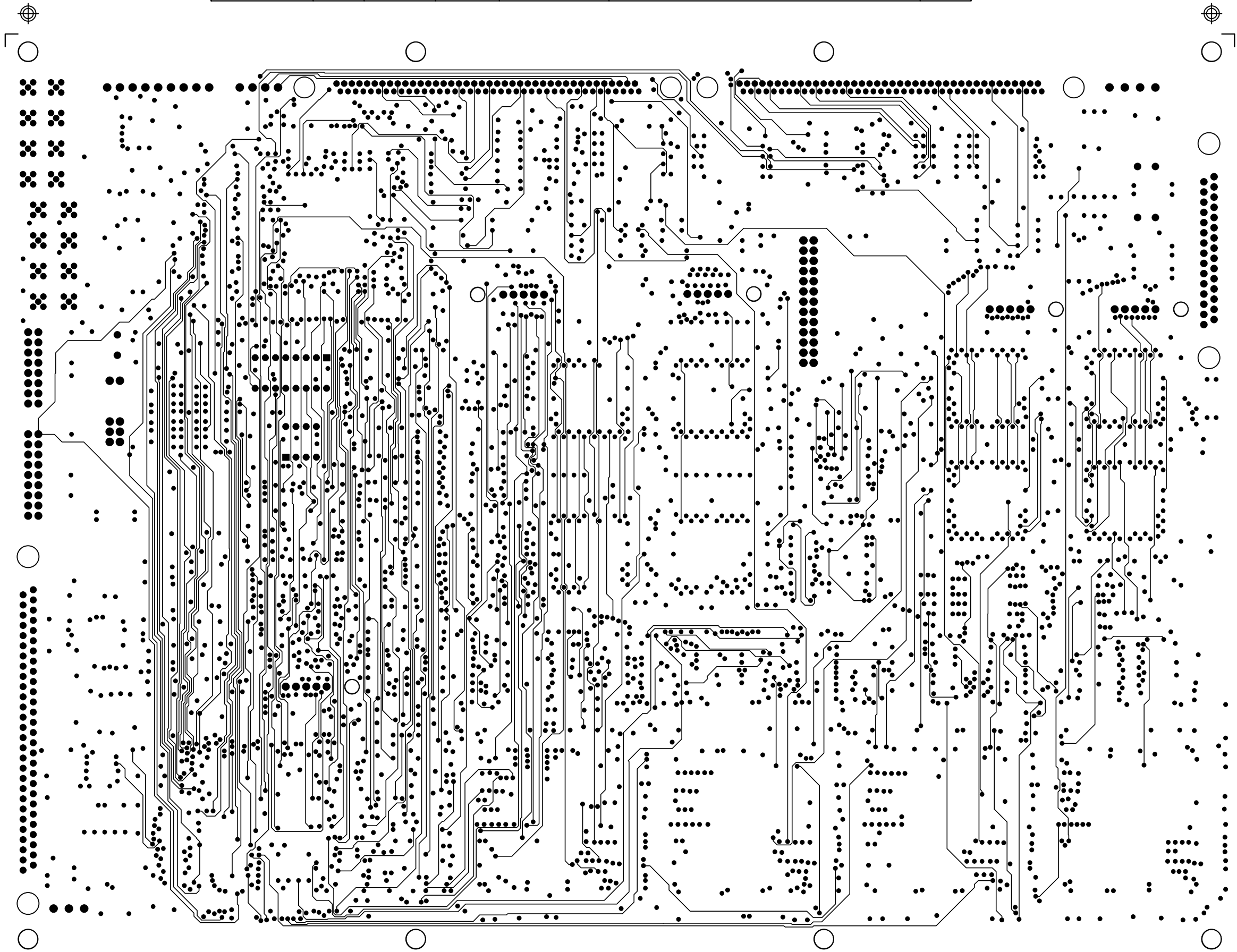
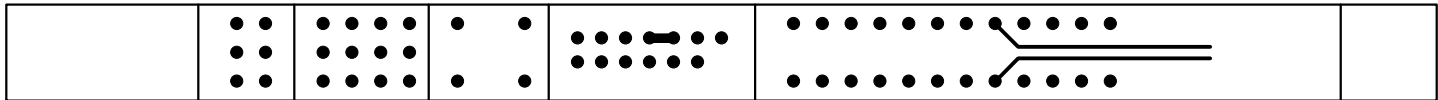
YOUR COMPANY NAME			
ARTWORK / INTERNAL SIGNAL / LAYER 5			
TEST BOARD			
		NO.	#####
DATE: ##/##/##	REV. #	ARTWORK MASTER L5	



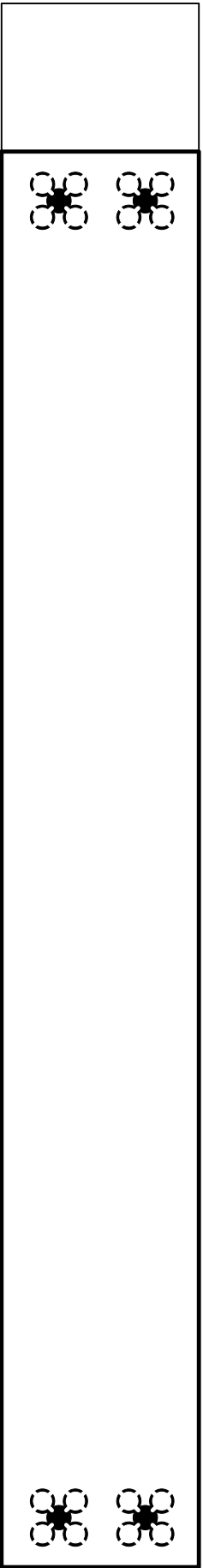
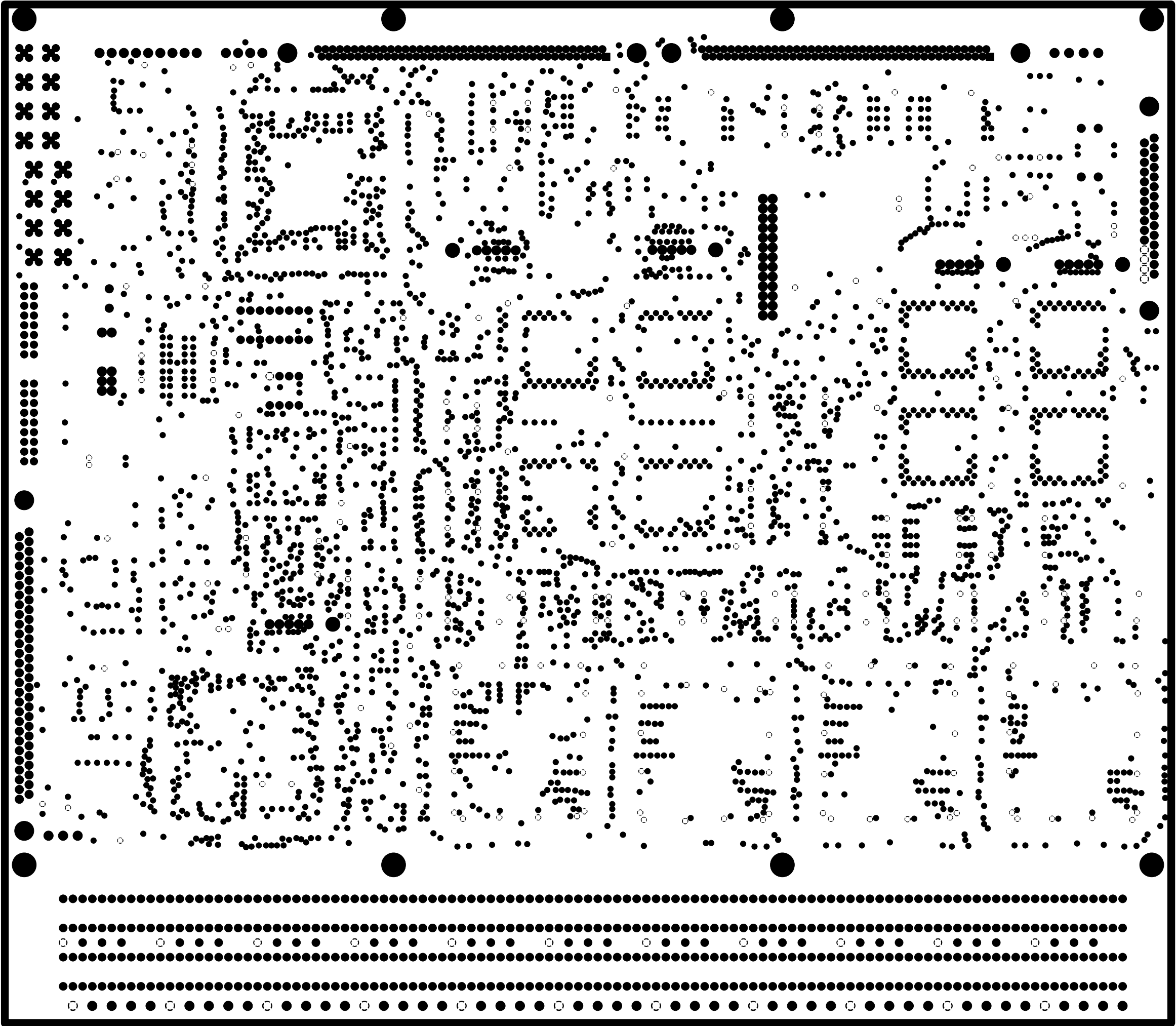
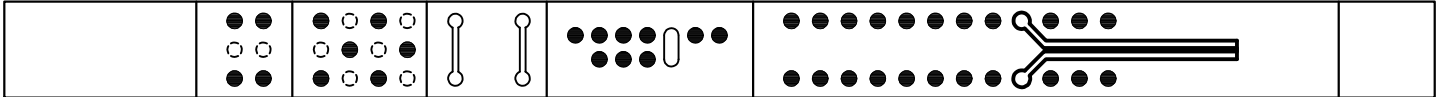
YOUR COMPANY NAME			
ARTWORK / IMBEDDED PLANE (GND) / LAYER 6			
TEST BOARD			
		NO.	#####
DATE: ##/##/##	REV. #	ARTWORK MASTER L6	



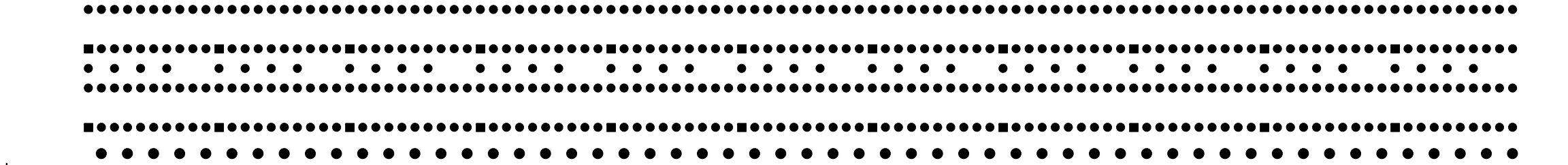
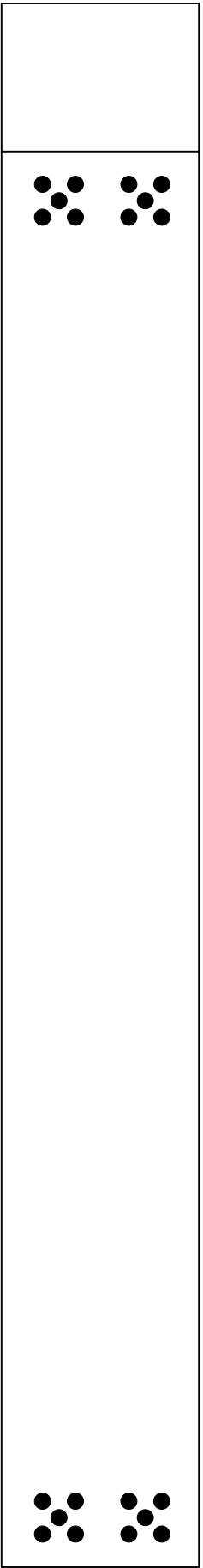
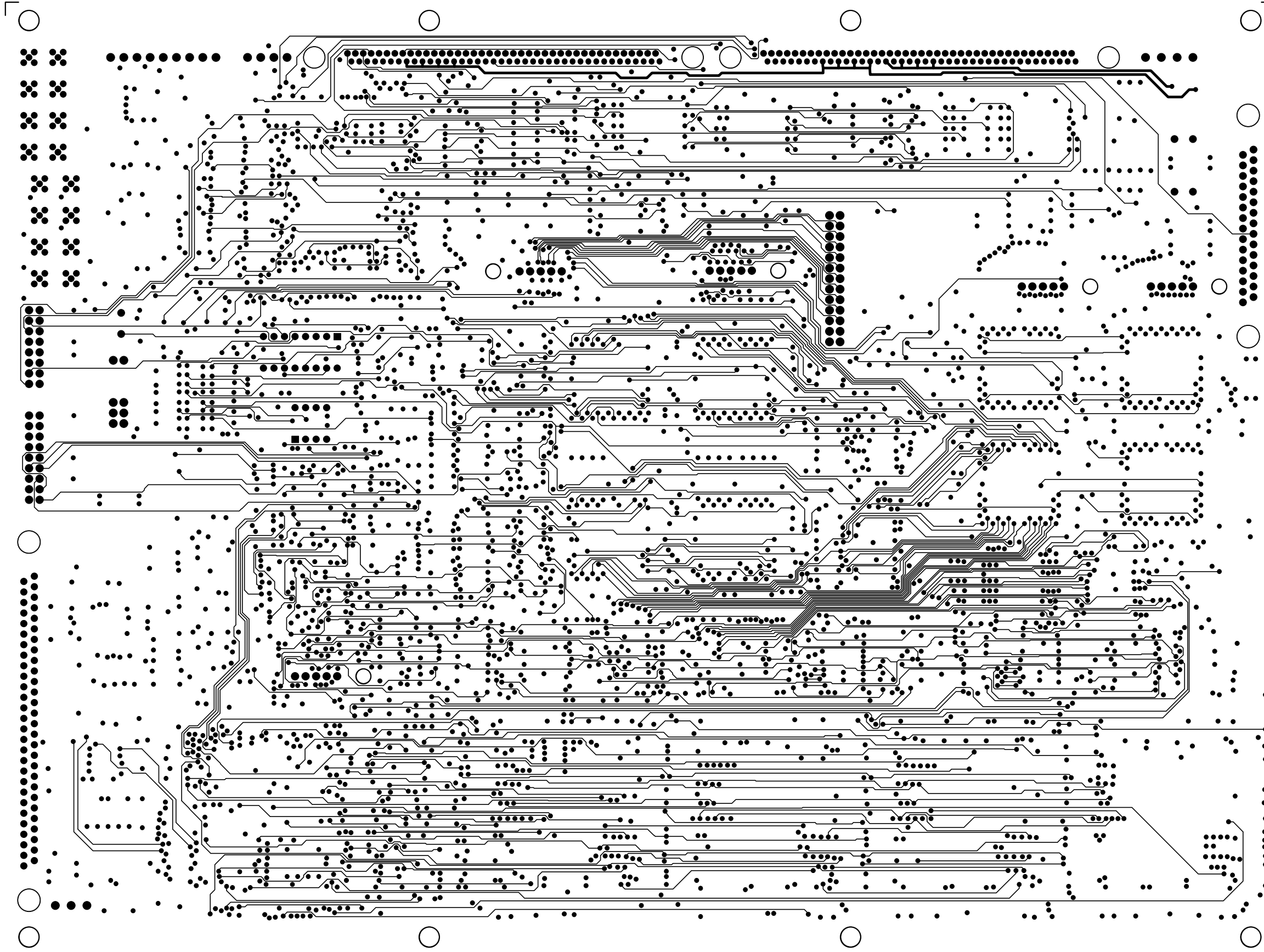
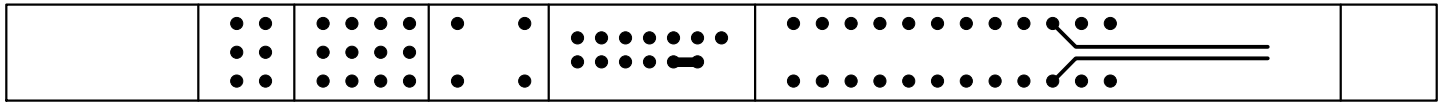
YOUR COMPANY NAME			
ARTWORK / IMBEDDED PLANE (VEE M5 2V) / LAYER 7			
TEST BOARD			
		NO.	#####
DATE: ##/##/##	REV. #	ARTWORK MASTER L7	



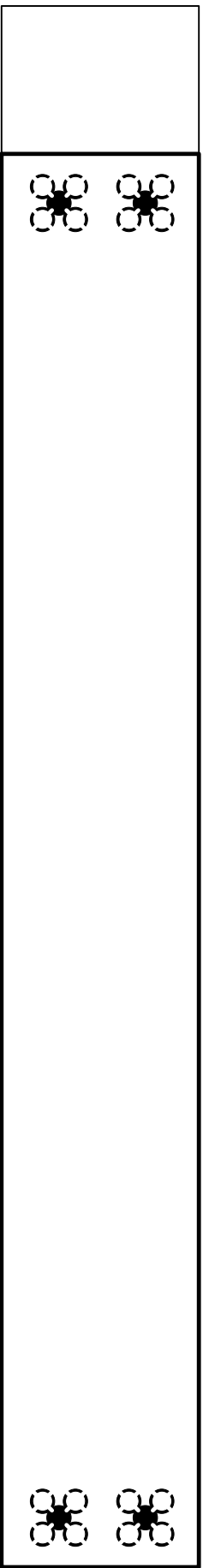
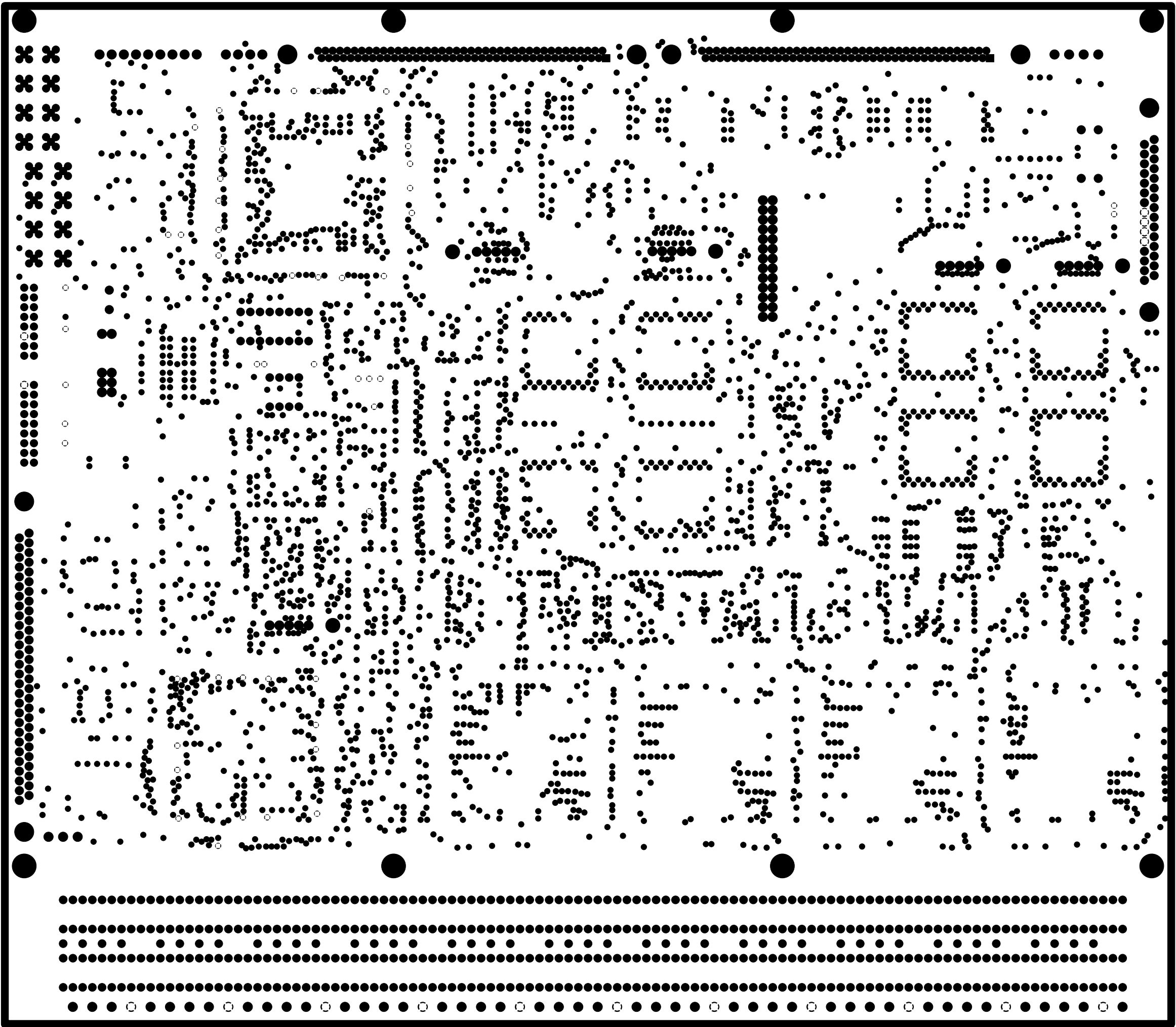
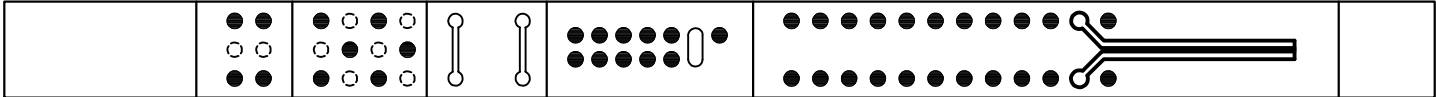
YOUR COMPANY NAME		
ARTWORK / INTERNAL SIGNAL / LAYER 8		
TEST BOARD		
		NO. #####
DATE: ##/##/##	REV. #	ARTWORK MASTER L8



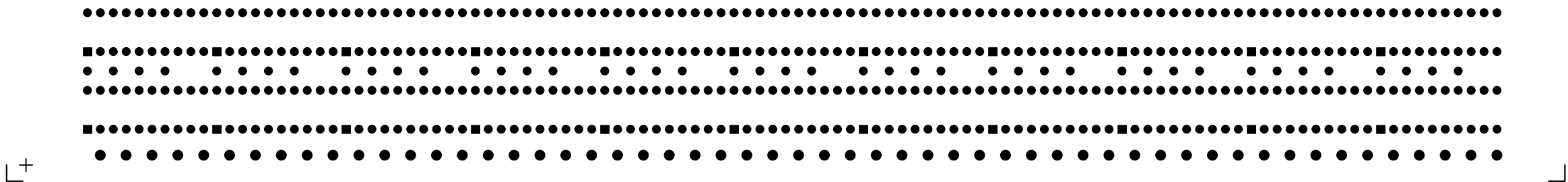
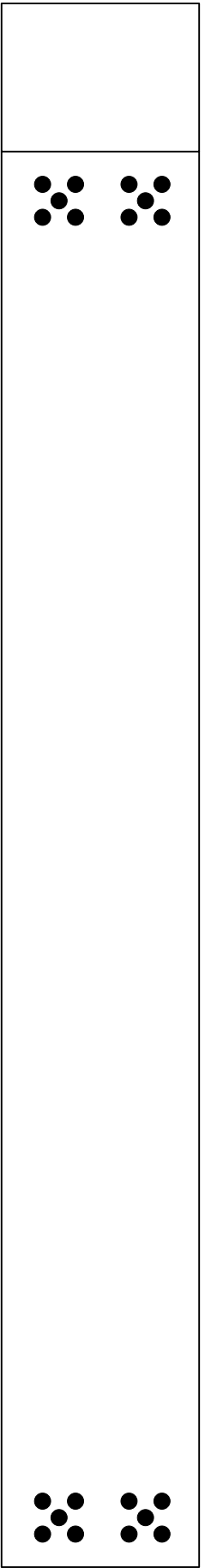
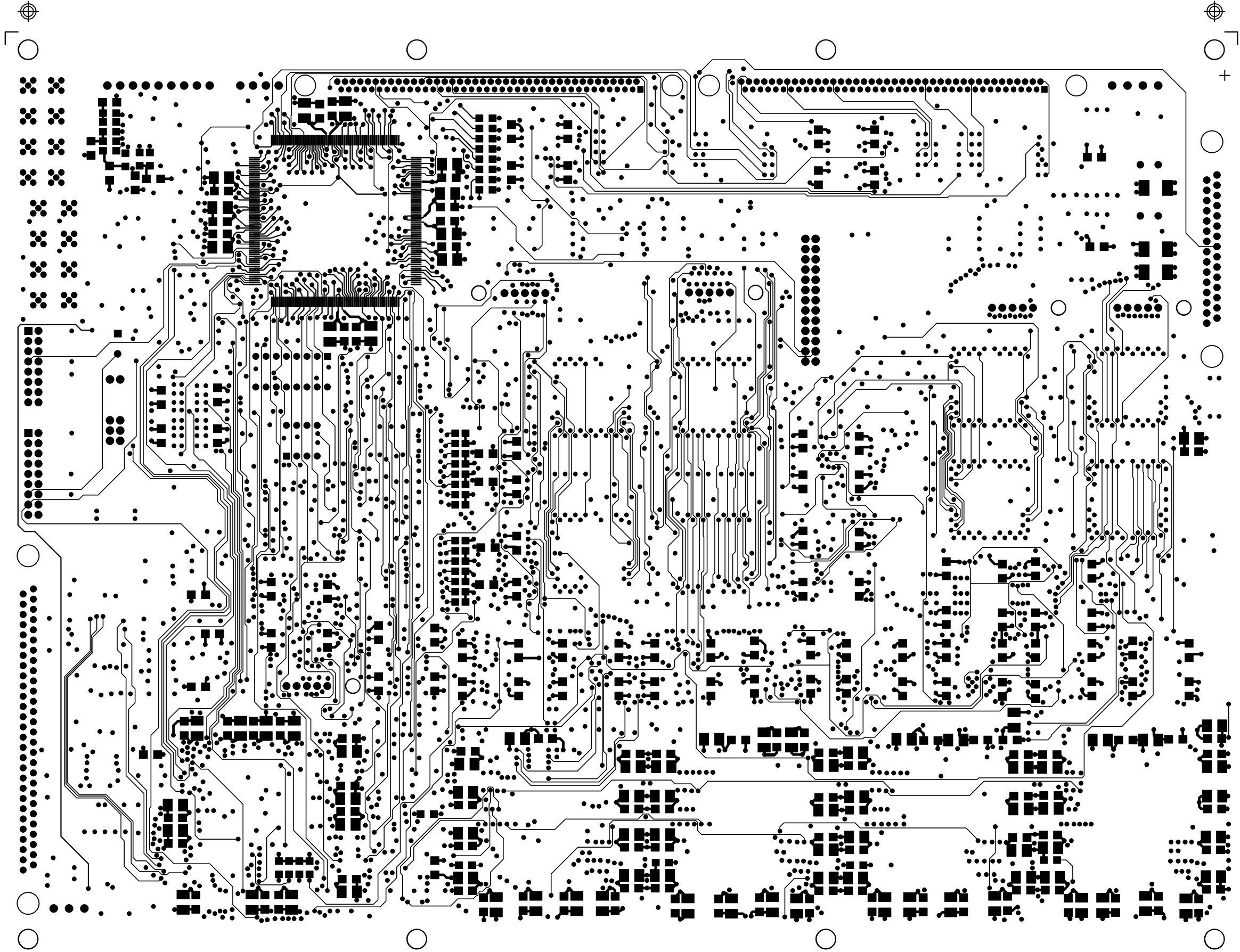
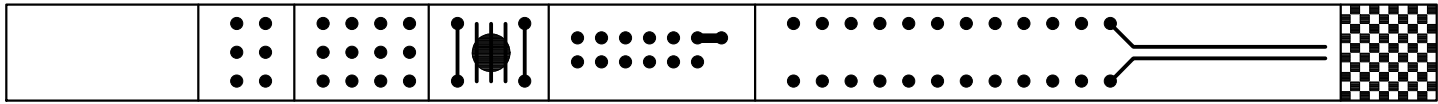
YOUR COMPANY NAME		
ARTWORK / IMBEDDED PLANE (VCC P5V) / LAYER 9		
TEST BOARD		
		NO. #####
DATE: ##/##/##	REV. #	ARTWORK MASTER L9



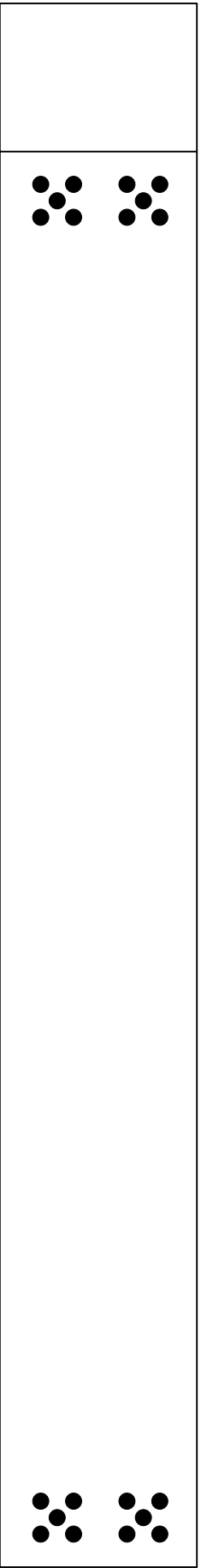
YOUR COMPANY NAME		
ARTWORK / INTERNAL SIGNAL / LAYER 10		
TEST BOARD		
		NO. #####
DATE: ##/##/##	REV. #	ARTWORK MASTER L10



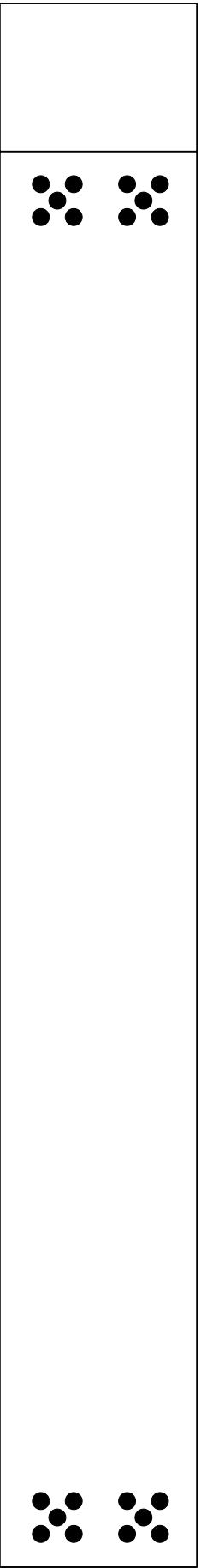
YOUR COMPANY NAME			
ARTWORK / IMBEDDED PLANE (VCC P3 3V) / LAYER 11			
TEST BOARD			
		NO.	#####
DATE: ##/##/##	REV. #	ARTWORK MASTER L11	



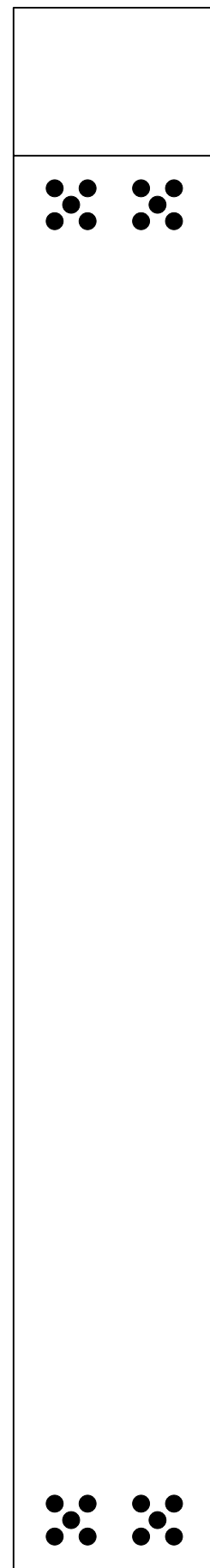
YOUR COMPANY NAME			
ARTWORK / SECONDARY SIDE / LAYER 12			
TEST BOARD			
		NO.	#####
DATE: ##/##/##	REV. #	ARTWORK MASTER L12	



YOUR COMPANY NAME		
TEST BOARD		
		NO. #####
DATE: ##/##/##	REV. #	

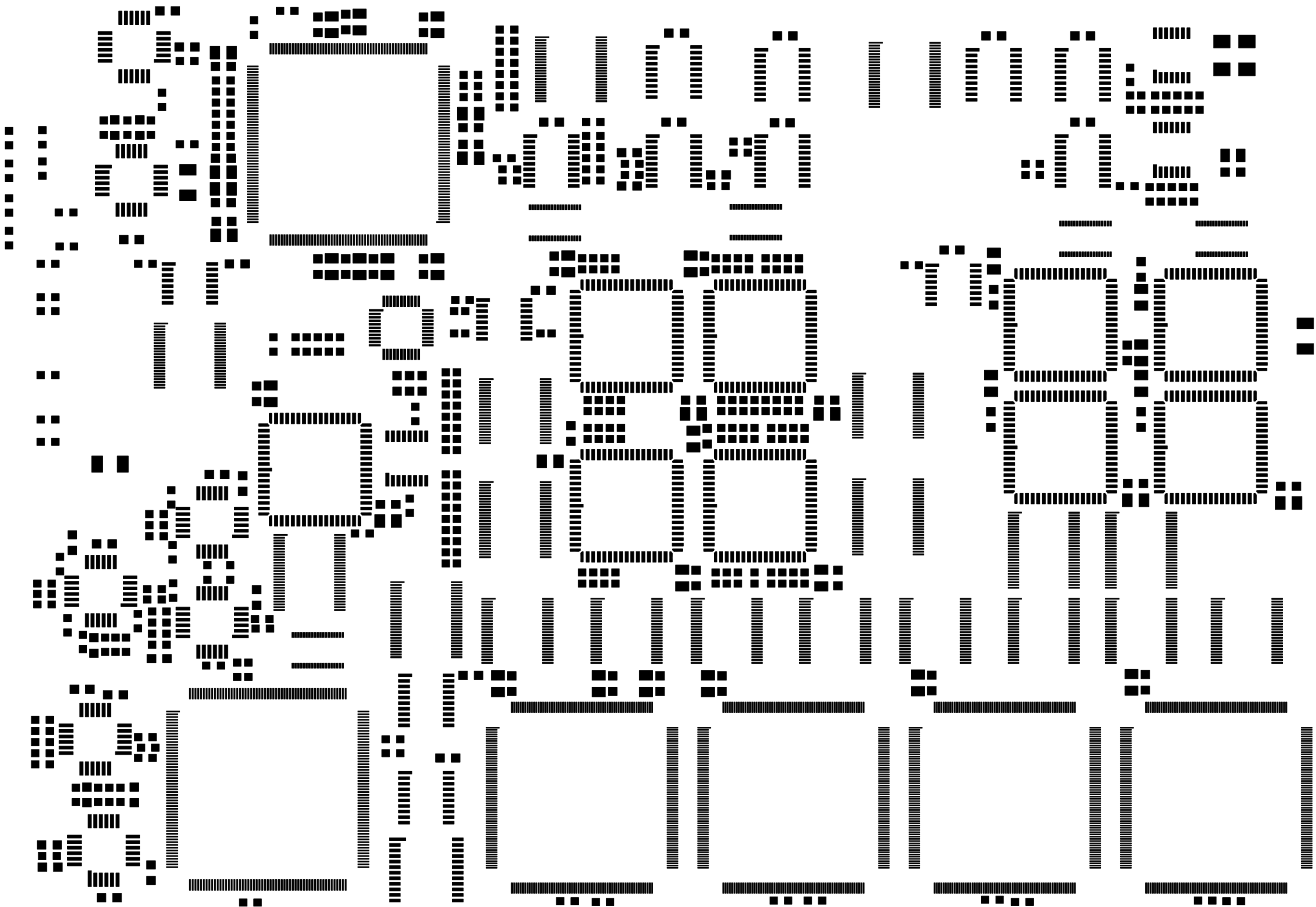


YOUR COMPANY NAME		
ARTWORK / PRIMARY SOLDER MASK TEST BOARD		
		NO. #####
DATE: ##/##/##	REV. #	SOLDER MASK L1



YOUR COMPANY NAME		
ARTWORK / SECONDARY SOLDER MASK TEST BOARD		
		NO. #####
DATE: ##/##/##	REV. #	SOLDER MASK L12

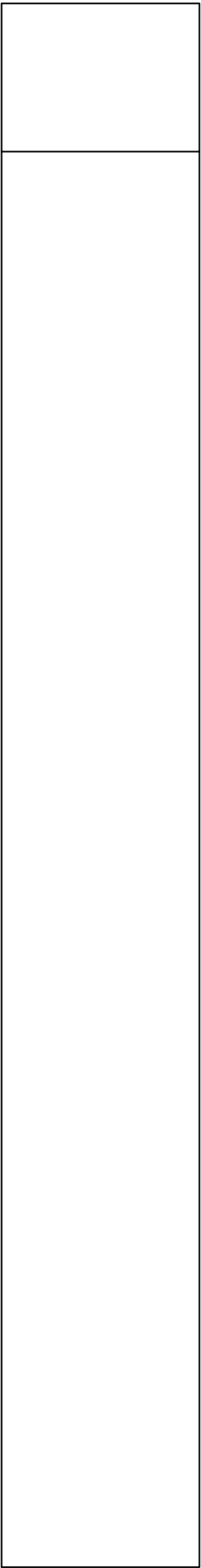
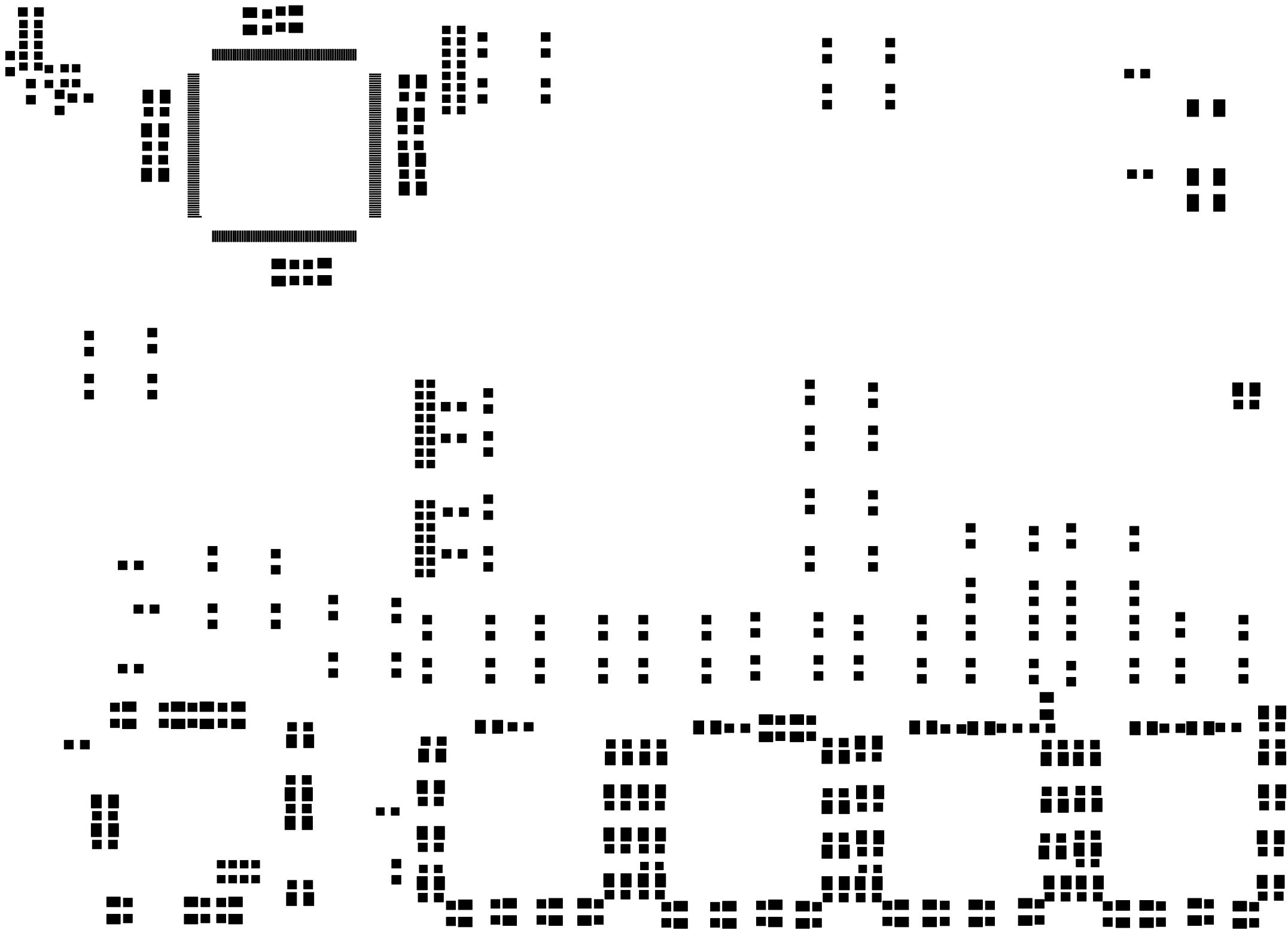
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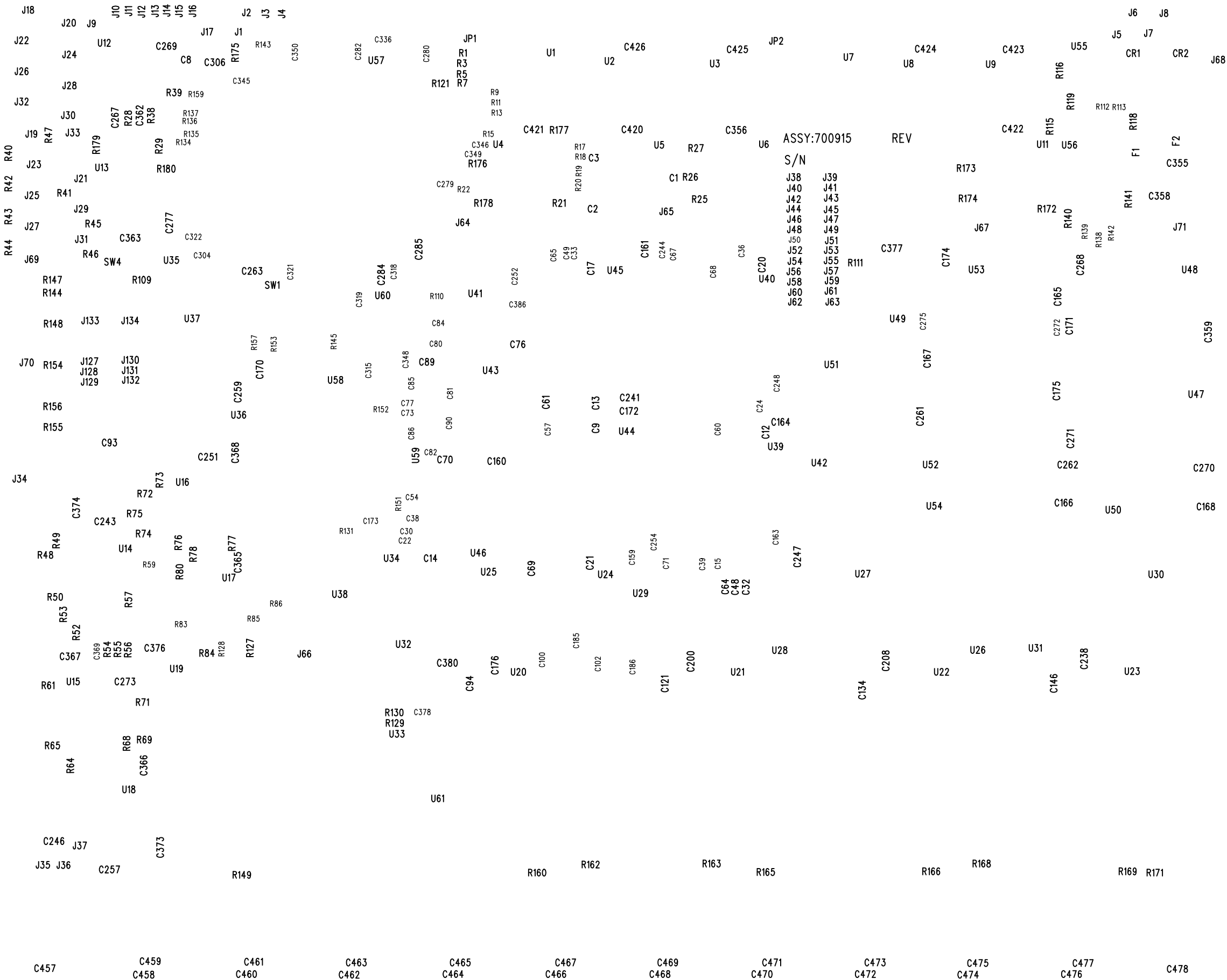
YOUR COMPANY NAME		
ARTWORK / PRIMARY SOLDER PASTE TEST BOARD		
	NO.	#####
DATE: ##/##/##	REV. #	SOLDER PASTE L1

REVERSE IMAGE	FOR SOLDER	PASTE MASK	
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YOUR COMPANY NAME		
ARTWORK / SECONDARY SOLDER PASTE TEST BOARD		
		NO. #####
DATE: ##/##/##	REV. #	SOLDER PASTE L12

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YOUR COMPANY NAME		
ARTWORK / SECONDARY SILKSCREEN TEST BOARD		
		NO. #####
DATE: ###/###/##	REV. #	SILK SCREEN L12

